

IN THE CLAIMS

What is claimed is:

1 1. A semiconductor integrated circuit device, comprising:
2 a plurality of insulated gate field effect transistors (IGFETs) coupled to
3 a corresponding input/output (I/O) terminal through a corresponding first
4 resistance;
5 a first clamping device coupled to each I/O terminal;
6 a second clamping circuit corresponding to each IGFET, each second
7 clamping circuit including a second clamping device and the corresponding
8 first resistance, each second clamping device having a first terminal connected
9 to a gate electrode of the corresponding IGFET and a second terminal
10 connected to a source/drain terminal of the corresponding IGFET and a supply
11 potential wiring;
12 each first clamping device being coupled to one second clamping
13 device through a second resistance; and
14 at least two of the second clamping circuits vary from one another.

1 2. The semiconductor integrated circuit device method of claim 1, wherein:
2 a supply potential wiring is selected from the group consisting of an
3 electric power supply potential wiring, a ground electric potential wiring, and a
4 substrate electric potential wiring.

1 3. The semiconductor integrated circuit device of claim 1, wherein:
2 the at least two second clamping circuits vary by the second clamping
3 device of one second clamping circuit having a different capability than the
4 second clamping device of the other second clamping circuit.

1 4. The semiconductor integrated circuit device of claim 1, wherein:
2 the at least two second clamping circuits vary by a first resistance (Rin) of
3 one second clamping circuit having a different value than the first resistance (Rin)
4 of the other second clamping circuit, and a ratio between the second resistance
5 and the first resistance (Rg/Rin) for both clamping circuits having a
6 predetermined maximum value.
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1 5. The semiconductor integrated circuit device of claim 1, wherein:
2 a length of a wiring that connects the second clamping devices to the
3 gate electrode of the corresponding IGFETs is no more than 100 micrometers.

1 6. The semiconductor integrated circuit device of claim 1, wherein:
2 a length of a wiring that connects the second clamping devices to the
3 source/drain electrode of the corresponding IGFETs is no more than 100
4 micrometers.

1 7. The semiconductor integrated circuit device of claim 1, wherein:
2 the first resistance comprises essentially a wiring resistance and a

3 contact resistance.

1 8. The semiconductor integrated circuit device of claim 1, wherein:
2 the majority of at least one first resistance includes non-wiring
3 structures.

1 9. The semiconductor integrated circuit device of claim 1, wherein:
2 at least one first resistance includes an effective channel resistance of
3 an input path IGFET.

1 10. The semiconductor integrated circuit device of claim 1, wherein:
2 the second resistance comprises essentially a supply potential wiring
3 resistance and a contact resistance where the first and second clamping
4 devices are connected to the supply potential wiring.

1 11. The semiconductor integrated circuit device of claim 1, wherein:
2 each first clamping devices has a first terminal connected to one of the
3 I/O terminals and a second terminal, the second terminals of each first
4 clamping device being connected to the second terminal of one of the second
5 clamping devices by system wiring of at least one supply terminal; and
6 the second resistance comprises essentially a contact resistance
7 between the second terminal of the first clamping device and the supply
8 potential wiring, a supply potential wiring between the first clamping device

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9 and the supply terminal, a supply terminal resistance, a supply potential
10 wiring between the supply terminal and the second terminal of the second
11 clamping device, and a contact resistance between the second terminal of the
12 second clamping device and the supply potential wiring.

1 12. The semiconductor integrated circuit device of claim 1, wherein:
2 each first clamping device has a first terminal connected to one of the
3 I/O terminals and a second terminal connected to a first supply terminal; and
4 the second terminal of each second clamping device is connected to a
second supply terminal different from the first supply terminal.

1 13. The semiconductor integrated circuit device of claim 12, wherein:
2 the first and second supply terminals are connected to one another
3 through a conductive integrated circuit package structure.

1 14. The semiconductor integrated circuit device of claim 1, wherein:
2 at least a portion of each second clamping device is selected from the
3 group consisting of an IGFET having a source/drain coupled to a gate, an
4 NPN bipolar device, a diode, and a thyristor.

1 15. The semiconductor integrated circuit device of claim 1, wherein:
2 the at least two second clamping circuits vary by the second clamping
3 device of one second clamping circuit having a different construction than the

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4 second clamping device of the other second clamping circuit.

1 16. A method for designing a protective circuit for a semiconductor integrated circuit
2 device that includes insulated gate field effect transistors (IGFETs) formed thereon, the
3 method comprising the steps of:

4 executing a simulation with a predetermined charged device model
5 (CDM) equivalent circuit that includes a first clamping device connected to an
6 input/output (I/O) terminal, a first IGFET having a gate connected to the I/O
7 terminal through a first resistance (R_{in}), a second clamping device connected
8 between gate and source/drain terminals of the first IGFET and connected to a
9 supply potential wiring, the first and second clamping devices being
10 connected to one another through a second resistance (R_g); and

11 selecting a ratio of the second resistance and the first resistance
12 (R_g/R_{in}) that prevents a potential between the gate and source/drain terminal
13 of the first IGFET from exceeding a predetermined value.

1 17. The method of claim 16, wherein:

2 the predetermined value is determined from a relationship between
3 CDM test results and ratios of the second resistance and the first resistance
4 (R_g/R_{in}), and simulation results showing a relationship between a potential
5 between the gate and source/drain terminal of the first IGFET and ratios of the
6 second resistance and the first resistance (R_g/R_{in}).

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1 18. The method of claim 16, wherein:

2 the first and second resistance values are set to ranges that ensure
3 predetermined circuit characteristics.

1 19. The method of claim 16, further including:

2 changing the properties a second clamping device for a second IGFET
3 to prevent a potential between the gate and source/drain terminal of the first
4 IGFET from exceeding a predetermined value.

1 20. The method of claim 19, wherein:

2 the changing the properties of the second clamping device includes
3 changing the size of the second clamping device.